TS60GSSD25D-M
TS120GSSD25D-M

2.5” Solid State Drive

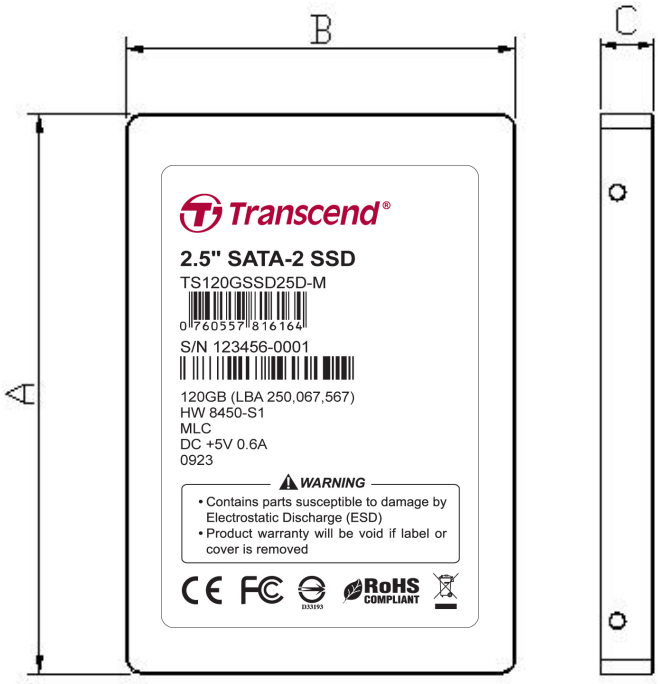
Description

Transcend 2.5” SATA II solid state drive is a huge capacity, high speed, and low power consumption without moving parts which design for take the place of traditional hard disk drive. It provides fast read and write performance for high end system such as server and storage system. Build in advance ECC and global wear-leveling provide a durable solution is perfect replacement storage device for Server systems, Storage systems, PCs, Laptops and gaming systems.

Features

- Fully SATA II 3.0Gbps compatible
- Non-volatile Flash Memory for outstanding data retention
- Built-in 64MB DRAM cache buffer
- Built-in ECC (Error Correction Code) functionality and wear-leveling algorithm ensures highly reliable of data transfer
- Lower Power Consumption
- Shock resistance

Placement



Dimensions

Side	Millimeters	Inches
A	100.00 ± 0.40	3.937 ± 0.016
B	69.85 ± 0.20	2.750 ± 0.008
C	9.50 ± 0.20	0.374 ± 0.008

Specifications

Physical Specification		
Form Factor		2.5-inch HDD
Storage Capacities		60GB and 120GB
Dimensions (mm)	**Length**	100.00 ± 0.40
	Width	69.85 ± 0.20
	Height	9.50 ± 0.20
Input Voltage		5V ± 5%
Weight		91g ± 2g
Connector		SATA 7+15 pins combo connector

Environmental Specifications	
Operating Temperature	0 ℃ to 70 ℃
Storage Temperature	- 40 ℃ to 85 ℃

Power Requirements			
Input Voltage		5V ± 5% @25℃	
Mode		**Max. (mA)**	**Max. (W)**
Power Consumption (60GB)	**Write**$_{(peak)}$	395.6	1.98
	Read$_{(peak)}$	176.7	0.88
	Idle$_{(peak)}$	88.3	0.44
Power Consumption (120GB)	**Write**$_{(peak)}$	534.9	2.67
	Read$_{(peak)}$	196.9	0.98
	Idle$_{(peak)}$	88.3	0.44

Performance		
Model P/N	**Sequential Read**$_{(Max.)}$	**Sequential Write**$_{(Max.)}$
TS60GSSD25D-M	210 MB/s	150 MB/s
TS120GSSD25D-M	230 MB/s	180 MB/s

Actual Capacity				
Model P/N	**User Max. LBA**	**Cylinder**	**Head**	**Sector**
TS60GSSD25D-M	125,045,424	7,783	255	63
TS120GSSD25D-M	250,067,567	15,565	255	63

Reliability	
Data Reliability	Supports BCH ECC 8 ,12 or 16bits/sector
Data Retention	10 years
MTBF	1.5M hours
Endurance	60GB: 75.7 years @ 20GB write/day 120GB: 151.4 years @ 20GB write/day

Vibration	
Operating	5.0G, 15 – 800Hz
Non-Operating	5.0G, 15 – 800Hz

* Note: Reference to the IEC 60068-2-6 Testing procedures; Operating-Sine wave, 5-800Hz/1 oct., 1.5mm, 3g, 0.5 hr./axis, total 1.5 hrs.

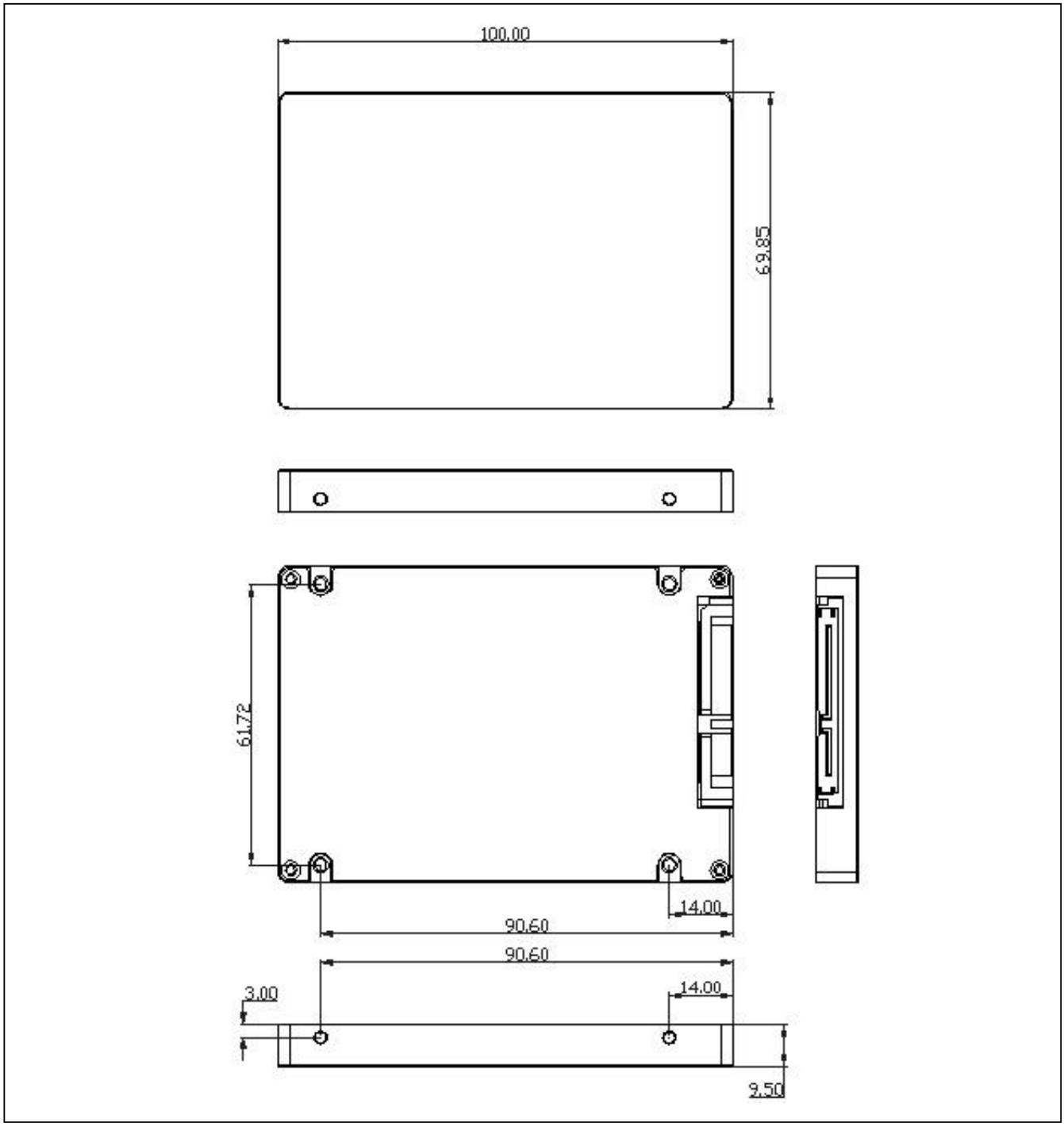
Shock	
Operating	1500G, 0.5ms
Non-Operating	1500G, 0.5ms

* Note: Reference to the IEC 60068-2-27 Testing procedures; Operating-Half-sine wave, 1500g, 0.5ms, 3 times/dir., total 18 times.

Regulations	
Compliance	CE, FCC and BSMI

Package Dimensions

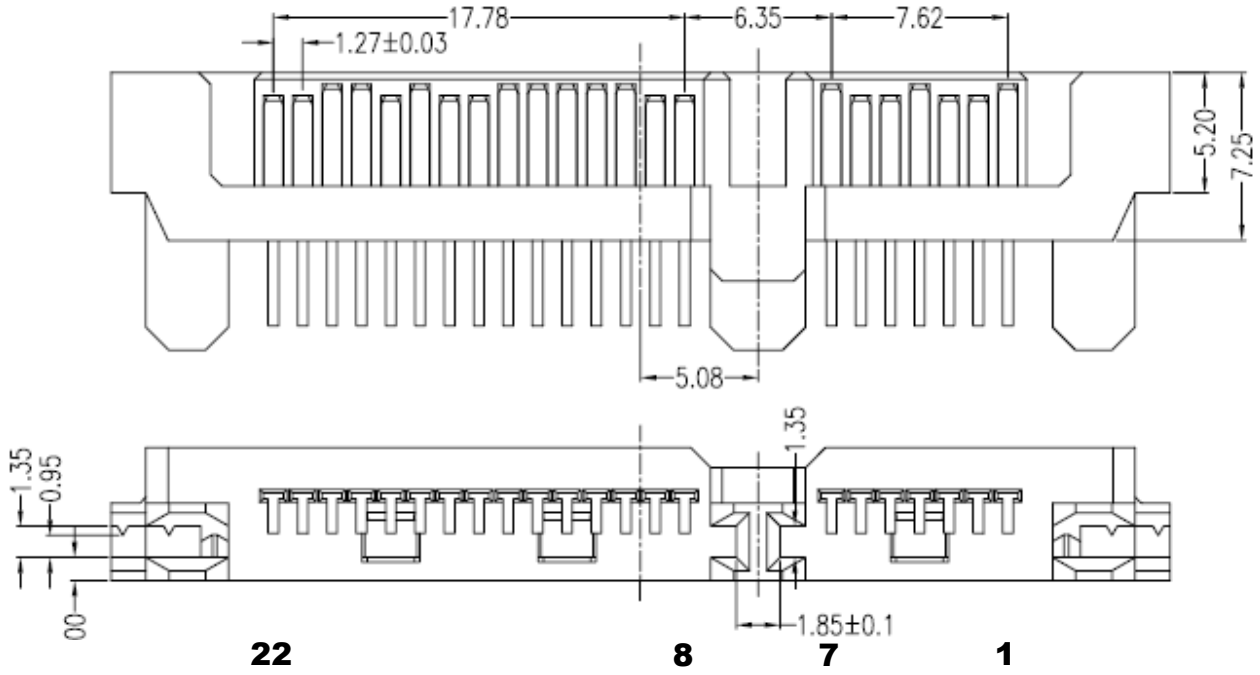
Below figure illustrates the Transcend 2.5” SATA Solid State Drive. All dimensions are in mm.



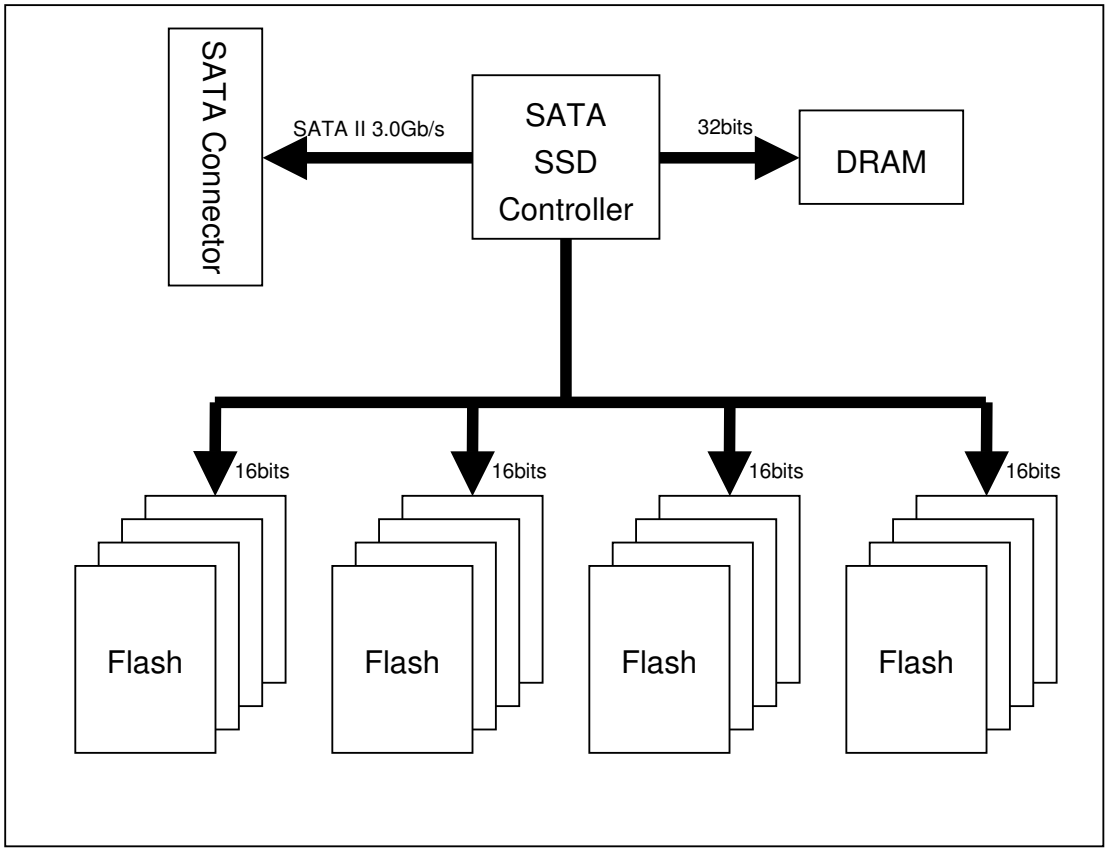
Pin Assignments

Pin No.	Pin Name	Pin No.	Pin Name
01	GND	02	A+
03	A-	04	GND
05	B-	06	B+
07	GND	08	NC
09	NC	10	NC
11	GND	12	GND
13	GND	14	5V
15	5V	16	5V
17	GND	18	DAS/DSS
19	GND	20	NC
21	NC	22	NC

Pin Layout



Block Diagram



Reliability

Wear-Leveling algorithm

The controller supports static/dynamic wear leveling. When the host writes data, the controller will find and use the block with the lowest erase count among the free blocks. This is known as dynamic wear leveling. When the free blocks' erase count is higher than the data blocks', it will activate the static wear leveling, replacing the not so frequently used user blocks with the high erase count free blocks.

ECC algorithm

The controller use Reed Solomon code or BCH code option

Reed Solomon: 6Bytes/sector for 128Bytes spare and 12Bytes/sector for 218Bytes spare

BCH: 8 or 12 bits/sector for 128Bytes spare and 16bits/sector for 218Bytes spare size

Bad-block management

When the flash encounters ECC failed, program fail or erase fail, the controller will mark the block as bad block to prevent the used of this block and caused data lost later on.

Supported ATA Command Lists

Command Name	Command Code (Hex)	Command Name	Command Code (Hex)
CHECK POWER MODE	E5h or 98h	Disable write cache	EFh/82h
DEVICE CONFIGURATION	-	Set transfer mode	EFh/03h
DEVICE CONFIGURATION FREEZE LOCK	B1h/C1h	Enable DMA Setup FIS Auto-Activate optimization	EFh/10h/02h
DEVICE CONFIGURATION IDENTIFY	B1h/C2h	Disable DMA Setup FIS Auto-Activate optimization	EFh/90h/02h
DEVICE CONFIGURATION RESTORE	B1h/C0h	Enable Device-initiated interface power state transitions	EFh/10h/03h
DEVICE CONFIGURATION SET	B1h/C3h	Disable Device-initiated interface power state transitions	EFh/10h/03h
DOWNLOAD MICROCODE	92h	SET MAX	-
EXECUTE DEVICE DIAGNOSTIC	90h	SET MAX ADDRESS	F9h/na
FLUSH CACHE	E7h	SET MAX FREEZE LOCK	F9h/04h
FLUSH CACHE EXT	EAh	SET MAX LOCK	F9h/02h
IDENTIFY DEVICE	ECh	SET MAX SET PASSWORD	F9h/01h
IDLE	E3h or 97h	SET MAX UNLOCK	F9h/03h
IDLE IMMEDIATE	E1h or 95h	SET MAX ADDRESS EXT	37h
INITIALIZE DEVICE PARAMETERS	91h	SET MULTIPLE MODE	C6h
NOP	00h/00h	SLEEP	E6h or 99h
READ BUFFER	E4h	SMART	-
READ DMA	C8h	SMART DISABLE OPERATIONS	B0h/D9h
READ DMA EXT	25h	SMART ENABLE OPERATIONS	B0h/D8h
READ FPDMA QUEUED	60h	SMART ENABLE/DISABLE AUTOMATIC OFF-LINE	B0h/DBh
READ LOG EXT	2Fh	SMART EXECUTE OFF-LINE IMMIDIATE	B0h/D4h
READ MULTIPLE	C4h	SMART READ DATA	B0h/D0h
READ MULTIPLE EXT	29h	SMART READ LOG	B0h/D5h
READ NATIVE MAX ADDRESS	F8h	SMART RETURN STATUS	B0h/DAh
READ NATIVE MAX ADDRESS EXT	27h	SMART SAVE ATTRIBUTE VALUES	B0h/D3h
READ SECTOR(S)	20h	SMART WRITE LOG	B0h/D6h
READ SECTOR(S) EXT	24h	STANDBY	E2h or 96h
READ VERIFY SECTOR(S)	40h	STANDBY IMMEDIATE	E0h or 94h
READ VERIFY SECTOR(S) EXT	42h	WRITE BUFFER	E8h
SECURITY DISABLE PASSWORD	F6h	WRITE DMA	CAh
SECURITY ERASE PREPARE	F3h	WRITE DMA EXT	35h
SECURITY ERASE UNIT	F4h	WRITE FPDMA QUEUED	61h
SECURITY FREEZE LOCK	F5h	WRITE LOG EXT	3Fh
SECURITY SET PASSWORD	F1h	WRITE MULTIPLE	C5h
SECURITY UNLOCK	F2h	WRITE MULTIPLE EXT	39h
SEEK	70h	WRITE SECTOR(S)	30h
SET FEATURES	-	WRITE SECTOR(S) EXT	34h
Enable write cache	EFh/02h		

SMART

SMART subcommand sets

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the SMART Function Set command. The subcommands are listed below.

Command	Command Code (Hex)
SMART READ DATA	D0h
SMART SAVE ATTRIBUTE VALUES	D3h
SMART EXECUTE OFF-LINE IMMIDIATE	D4h
SMART READ LOG	D5h
SMART WRITE LOG	D6h
SMART ENABLE OPERATIONS	D8h
SMART DISABLE OPERATIONS	D9h
SMART RETURN STATUS	DAh
SMART ENABLE/DISABLE AUTOMATIC OFF-LINE	DBh

SMART Read Data (subcommand D0h)

This subcommand returns the device's Attribute Values to the host. The Attribute Values consist of 512bytes.

Device Attribute Data Structure

Byte	Description
0~1	Data structure revision number (Vendor Specific)
2~361	1st - 30th Individual attribute data (Vendor Specific)
362	Off-line data collection status
363	Self-test execution status
364~365	Total time in seconds to complete off-line data collection activity
366	Vendor Specific
367	Off-line data collection capability
368-369	SMART capability
370	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	Self-test failure check point (Vendor Specific)
372	Short self-test routine recommended polling time(in minutes)
373	Extended self-test routine recommended polling time(in minutes)
374-510	Reserved
511	Data structure checksum

Individual Attribute Data Structure

Byte	Description
0	Attribute ID Number
1~2	Status Flag
3~10	Attribute Value (FFFF FFFF FFFF FFFFh)
11	Reserved

Attribute ID Numbers

ID	Attribute Name	ID	Attribute Name
1	Raw Read Error Rate *	200	Total Count of Read Commands
9	Power-On Hours	201	Total Count of Write Commands
12	Power Cycle Count	202	Total Count of Error Bits from Flash
184	Initial Bad Block Count	203	Total Count of Read Sectors with Correctable Bit Errors
195	Program Failure Block Count	204	Bad Block Full Flag
196	Erase Failure Block Count	205	Maximum PE Count Specification
197	Read Failure Block Count (Uncorrectable Bit Errors)	206	Minimum Erase Count
198	Total Count of Read Sectors	207	Maximum Erase Count
199	Total Count of Write Sectors	208	Average Erase Count

* indicates that the corresponding Attribute Values is fixed value for compatibility.

SMART Save Attribute Values (subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Autosave feature.

SMART Execute Off-line Immediately (subcommand D4h)

This subcommand causes the device to start the off-line process for the requested mode and operation. The LBA Low register shall be set to specify the operation to be executed.

SMART Read Log Sector (subcommand D5h)

This command returns the specified log sector content to the host. LBA Low and Sector Count registers shall be set to specify the log sector and sector number to be written.

Log Sector Address	No. Sector	Content	
00h	1	Log directory	Read Only
01h	1	SMART error log	Read Only
02h	1	Comprehensive SMART error log	Read Only
04h-05h	-	Reserved	Read Only
06h	1	SMART self-test log	Read Only
08h	-	Reserved	Read Only
09h	1	Selective self-test log	Read and Write
0Ah-7Fh	-	Reserved	Read Only
80h-9Fh	16	Host vendor specific	Read and Write
A0h-FFh	-	Reserved	Vendor Specific

SMART Log Directory

Byte	Description
0~1	SMART Logging Version (set to 01h)
2	Number of sectors in the log at log address 1
3	Reserved
4	Number of sectors in the log at log address 2
5	Reserved
...	
510	Number of sectors in the log at log address 255
511	Reserved

SMART summary error log sector

Byte	Description
0	SMART error log version (set to 01h)
1	Error log index
2~91	First error log data structure
92~181	Second error log data structure
182~271	Third error log data structure
272~361	Fourth error log data structure
362~451	Fifth error log data structure
452~453	Device error count
454~510	Reserved
511	Data Structure checksum

Error log data structure

Byte	Description
n ~ n+11	First command data structure
n+12 ~ n+23	Second command data structure
n+24 ~ n+35	Third command data structure
n+36 ~ n+47	Fourth command data structure
n+48 ~ n+59	Fifth command data structure
n+60 ~ n+89	Error data structure

Command data structure

Byte	Description
n	Content of the Device Control register when the Command register was written
n+1	Content of the Features Control register when the Command register was written
n+2	Content of the Sector Count Control register when the Command register was written
n+3	Content of the LBA Low register when the Command register was written
n+4	Content of the LBA Mid register when the Command register was written
n+5	Content of the LBA High register when the Command register was written
n+6	Content of the Device/Head register when the Command register was written
n+7	Content written to the Command register
n+8	Timestamp
n+9	Timestamp
n+10	Timestamp
n+11	Timestamp

Error data structure

Byte	Description
n	Reserved
n+1	Content written to the Error register after command completion occurred.
n+2	Content written to the Sector Count register after command completion occurred.
n+3	Content written to the LBA Low register after command completion occurred.
n+4	Content written to the LBA Mid register after command completion occurred.
n+5	Content written to the LBA High register after command completion occurred.
n+6	Content written to the Device/Head register after command completion occurred.
n+7	Content written to the Status register after command completion occurred.
n+8 – n+26	Extended error information
n+27	State
n+28	Life Timestamp (least significant byte)
n+29	Life Timestamp (most significant byte)

State field values

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
3h	xActive/Idle with BSY cleared to zero
x4h	Executing SMART off-line or self-test
x5h-xAh	Reserved
xBh-xFh	Vendor unique

Self-test log structure

Byte	Description
0~1	Data structure revision
n*24+2	Self-test number
n*24+3	Self-test execution status
n*24+4~n*24+5	Life timestamp
n*24+6	Self-test failure check point
n*24+7~n*24+10	LBA of first failure
n*24+11~n*24+25	Vendor specific
.....	.....
506~507	Vendor specific
508	Self-test log pointer
509~510	Reserved
511	Data structure checksum

N is 0 through 20.

The data structure contains the descriptor of the Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable to contain up to 21 descriptors. After 21 descriptors has been recorded, the oldest descriptor will be overwritten with the new descriptor. The self-test log pointer points to the most recent descriptor. When there is no descriptor, the value is 0. When there are descriptor(s), the value is 1 through 21.

Selective self-test log structure

Byte	Content	
0-1	Data structure revision	Read and Write
2-9	Starting LBA for test span 1	Read and Write
10-17	Ending LBA for test span 1	Read and Write
18-25	Starting LBA for test span 2	Read and Write
26-33	Ending LBA for test span 2	Read and Write
34-41	Starting LBA for test span 3	Read and Write
42-49	Ending LBA for test span 3	Read and Write
50-57	Starting LBA for test span 4	Read and Write
58-65	Ending LBA for test span 4+	Read and Write
66-73	Starting LBA for test span 5	Read and Write
74-81	Ending LBA for test span 5	Read and Write
82-337	Reserved	Reserved
338-491	Vendor specific	Vendor specific
492-499	Current LBA under test	Read
500-501	Current span under test	Read
502-503	Feature flags R/W	Read and Write
504-507	Vendor Specific	Vendor specific
508-509	Selective self test pending time	Read and Write
510	Reserved	Reserved
511	Data structure checksum	Read and Write

SMART Write Log Sector (subcommand D6h)

This command writes 512 bytes of data to the specified log sector. LBA Low and Sector Count registers shall be set to specify the log address and sector number to be written.

SMART Enable Operations (subcommand D8h)

This subcommand enables access to all SMART capabilities. Prior to receipt of a SMART Enable Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of SMART—either enabled or disabled—will be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART Enable Operations subcommands will not affect any of the Attribute Values.

SMART Disable Operations (subcommand D9h)

This subcommand disables all SMART capabilities. After receipt of this subcommand the device disables all SMART operations. Non self-preserved Attribute Values will no longer be monitored. The state of SMART—either enabled or disabled—is preserved by the device across power cycles. Note that this subcommand does not preclude the device's power mode attribute auto saving.

After receipt of the SMART Disable Operations subcommand from the host, all other SMART subcommands except SMART Enable Operations are disabled and will be aborted by the device returning the error code as specified in “SMART Error Codes”.

Any Attribute Values accumulated and saved to volatile memory prior to receipt of the SMART Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a SMART Read Attribute Values or a SMART Save Attribute Values command.

SMART Return Status (subcommand DAh)

This subcommand is used to communicate the reliability status of the device to the host's request. Upon receipt of the SMART Return Status subcommand the device saves any updated Attribute Values to the reserved sector, and compares the updated Attribute Values to the Attribute Thresholds.

SMART Enable/Disable Automatic Off-line (subcommand DBh)

This subcommand enables and disables the optional feature that cause the device to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then save this data to the device's nonvolatile memory. This subcommand may either cause the device to automatically initiate or resume performance of its off-line data collection activities or cause the automatic off-line data collection feature to be disabled. This subcommand also enables and disables the off-line read scanning feature that cause the device to perform the entire read scanning with defect reallocation as the part of the off-line data collection activities. The Sector Count register shall be set to specify the feature to be enabled or disabled:

Sector Count	Feature Description
00h	Disable Automatic Off-line
F8h	Enable Automatic Off-line

A value of zero written by the host into the device's Sector Count register before issuing this subcommand shall cause the automatic off-line data collection feature to be disabled. Disabling this feature does not preclude the device from saving attribute values to nonvolatile memory during some other normal operation such as during a power-on, during a power-off sequence, or during an error recovery sequence. A value of F8h written by the host into the device's Sector Count register before issuing this subcommand shall cause the automatic Off-line data collection feature to be enabled. Any other non-zero value written by the host into this register before issuing this subcommand is vendor specific and will not change the current Automatic Off-Line Data Collection and Off-line Read Scanning status. However, the device may respond with the error code specified in “SMART Error Codes”.

Security

Default setting

The Flash SSD is shipped with master password set to 20h value (ASCII blanks) and the lock function disabled. The system manufacturer/dealer may set a new master password by using the SECURITY SET PASSWORD command, without enabling the lock function.

Initial setting of the user password

When a user password is set, the drive automatically enters lock mode by the next powered-on.

SECURITY mode operation from power-on

In locked mode, the Flash SSD rejects media access commands until a SECURITY UNLOCK command is successfully completed.

Password lost

If the user password is lost and High level security is set, the drive does not allow the user to access any data. However, the drive can be unlocked using the master password.

If the user password is lost and Maximum security level is set, it is impossible to access data. However, the drive can be

unlocked using the ERASE UNIT command with the master password. The drive will erase all user data and unlock the drive.

SATA Optional Features

Power Segment Pin P11

Pin P11 of the power segment of the device connector may be used by the device to provide the host with an activity indication. The activity indication provided by pin P11 is primarily for use in backplane applications.

Asynchronous Signal Recovery

Phy may support asynchronous signal recovery for those applications where the usage model of device insertion into a receptacle (power applied at time of insertion) does not apply.

When signal is lost, both the host and the device may attempt to recover the signal. A host or device shall determine loss of signal as represented by a transition from PHYRDY to PHYRDYn, which is associated with entry into states LSI: NoCommErr or LS2:NoComm within the Link layer. Note that negation of PHYRDY does not always constitute a loss of signal. Recovery of the signal is associated with exit from state LS2:NoComm. If the device attempts to recover the signal before the host by issuing a COMINIT, the device shall return its signature following completion of the OOB sequence which included COMINIT. If a host supports synchronous signal recovery, when the host receives an unsolicited COMINIT, the host shall issue a COMRESET to the device. An unsolicited COMINIT is a COMINIT that was not in response to a preceding COMRESET, as defined by the host not being in the HP2:HR_AwaitCOMINIT state when the COMINIT signal is first received.

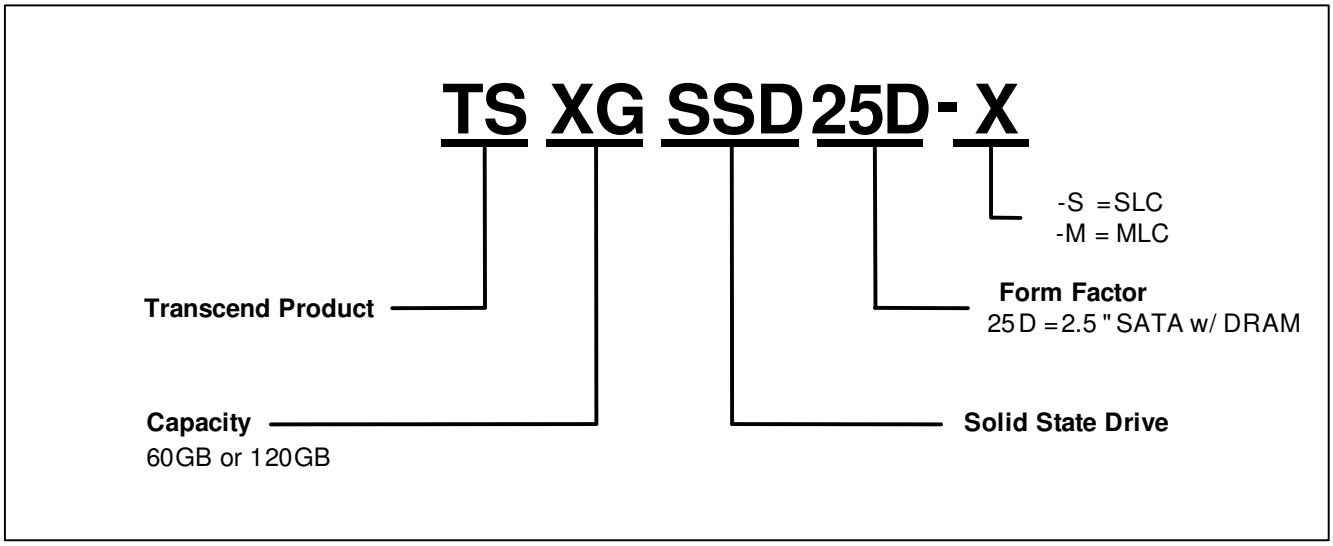
When a COMRESET is sent to the device in response to an unsolicited COMINIT, the host shall set the Status register to 7Fh and shall set all other Shadow Command Block Registers to FFh. When the COMINIT is received in response to the COMRESET which is associated with entry into state HP2B:HR_AwaitNoCOMINIT, the Shadow Status register value shall be updated to either FFh or 80h to reflect that a device is attached.

Identify Device Parameters

Word	Contents	Description
0	0C5Ah	General information
1	3FFFh	Number of logical cylinders
2	C837h	Specific configuration
3	0010h	Number of logical heads
4 – 5	0	Retired
6	003Fh	Number of logical sectors per logical track
7 – 8	0	Reserved
9	0000h	Retired
10 -19	XXXX	Serial number(20 ASCII characters)
20	0000h	Retired
21	FFFFh	Buffer Memory Size
22	3000h	Obsolete
23 - 26	XXXX	Firmware revision (8 ASCII characters)
27- 46	XXXX	Model number
47	8001h	Number of sectors on multiple commands
48	0000h	Reserved
49	2F00h	Capabilities
50	4000h	Capabilities
51 - 52	0200h	PIO Mode support
53	0007h	Reserved
54	3FFFh	Number of current logical cylinders
55	0010h	Number of current logical heads
56	003Fh	Number of current logical sectors per track
57	FC10h	Obsolete
58	00FBh	
59	0101h	Multiple sector setting
60	XXXXh	Total number of user addressable sectors (LBA mode only)
61	XXXXh	
62	0000h	Obsolete
63	0007h	Multi-word DMA transfer
64	0003h	Flow control PIO transfer modes supported
65	0078h	Minimum Multiword DMA transfer cycle time per word
66	0078h	Manufacturer’s recommended Multiword DMA transfer cycle time per word
67	0078h	Minimum PIO transfer cycle time without flow control
68	0078h	Minimum PIO transfer cycle time with IORDY flow control
69 - 74	0	Reserved
75	001Fh	Queue Depth
76	0506h	Serial ATA capability
77	0000h	Reserved
78	004Ch	Serial ATA features supported
79	0048h	Serial ATA features enabled
80	00E0h	Major Version Number
81	0000h	Minor Version Number

82	346Bh	Command sets supported
83	7D01h	Command sets supported
84	4022h	Command set/feature supported extension
85	3469h	Command set/feature enabled
86	3C01h	Command set/feature enabled
87	4022h	Command set/feature default
88	407Fh	Ultra DMA transfer
89	0000h	Time required for security erase unit completion
90	0000h	Time required for Enhanced security erase completion
91	0000h	Current advanced power management value
92	0000h	Master Password Revision Code
93	0000h	COMRESET result
94	0000h	Automatic acoustic management value
95	0000h	Stream minimum request size
96 - 99	0	Reserved
100 - 103	XXXX	Maximum user LBA for 48bit address feature set
104-105	0	Reserved
106	4000h	Physical sector size / logical sector size
107	0000h	Reserved
108 - 111	XXXX	Unique ID
112 - 116	0	Reserved
117 - 118	0	Words per logical sector
119 - 126	0	Reserved
127	0000h	Removable media status notification feature set supported
128	XXXXh	Security status
129 - 159	0	Undefined
160-254	0	Reserved
255	XXXXh	Integrity word

Ordering Information



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